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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/747,779	12/22/2000	Hong Koo Kim	000939073311	4408

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EXAMINER
PIZARRO CRESPO, MARCOS D

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 02/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/747,779	KIM, HONG KOO	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24 and 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *9* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Attorney's Docket Number: 00939-073311 US

Filing Date: 12/22/2000

Claimed Priority Dates: 3/29/2000 (Provisional 60/193,046)
12/27/1999 (Provisional 60/173,175)

Applicant(s): Kim

Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment in paper no. 10 filed on 12/16/2002.

Acknowledgment

1. The amendment in paper no. 10, filed on 12/16/2002, in response to the Office action in paper no. 8, mailed on 9/24/2002 has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-24 and 26.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-10, 14-22 are rejected under section 35 U.S.C. 103(a) as being unpatentable over Hirai (US 5955755) and Kirlin (US 5225561) and Hirai (US 5955755).

4. Hirai shows (see, *e.g.*, fig. 1) all aspects of the instant invention including a method for fabricating a non-volatile memory device, the method comprising:

- providing a substrate **1**

- forming an oxide layer **4** overlying the substrate **1**
- forming a buffer layer **5** overlying the oxide layer **4**
- forming a ferroelectric material **6** overlying the substrate **1**
- forming a gate layer **7** overlying the ferroelectric material **6** and a channel region
- forming a first source/drain region **2** adjacent to a first side of the channel region
- forming a second source/drain region **3** adjacent to a second side of the channel region

Hirai (col.7/ll.37-44) also heats the substrate in an oxidizing atmosphere at a temperature of from 650-750°C. Hirai, however, fails to disclose this treatment as an annealing step that will enhance the alignment of crystallites of the buffer layer. Nonetheless, annealing is a thermal treatment carried out in order to eliminate various weaknesses, or to produce other qualities in a material. As taught by Kirlin (col.35/ll.30-33) and Maiti (col.3/ll.33-36, col.4/ll.10-14), Hirai's heating step will remove the vacancies of the buffer layer. Although the prior art fails to explicitly describe that Hirai's heating step enhances the alignment of crystallites within the layer, it is obvious that Hirai's thermal treatment would have the same claimed benefits since the same annealing step is used.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art that Hirai's heat treatment is an annealing step for the buffer

layer, as taught by Kirlin and Maiti, that will reduce defects and enhance the alignment of crystallites within the layer.

5. Regarding claim 3, Hirai shows that the ferroelectric material may be a PZT-bearing compound (col.2/ll.40-43).

6. Regarding claim 4, Hirai shows that the buffer layer may be a magnesium-bearing compound (col.2/ll.39).

7. Regarding claim 5, Hirai shows that the buffer layer may be a magnesium-oxide layer, the magnesium-oxide layer being a barrier layer (col.2/ll.39, col.3/ll.7-10).

8. Regarding claim 6, Hirai shows that the ferroelectric material may have a thickness of less than about 1000 angstroms (col.4/ll.42).

9. Regarding claim 7, Hirai shows that the buffer layer may have a thickness of 20 nanometers (col.4/ll.13-14).

10. Regarding claim 8, Hirai shows that the ferroelectric material may have a thickness greater than 100 angstroms (col.4/ll.42).

11. Regarding claim 9, Hirai shows that the ferroelectric material may be PZT (col.4/ll.37).

12. Regarding claim 10, Hirai shows that the buffer layer is a barrier diffusion layer substantially preventing the diffusion between the ferroelectric material and the substrate (col.4/ll.62-67).

13. Regarding claim 14, Hirai shows that the ferroelectric material is highly oriented (col.4/ll.40-41, col.5/ll.48-52).

14. Regarding claims 15 and 16, Hirai (col.10/ll.17-18) shows that the ferroelectric material is a highly oriented film (001)-thin-film. The polycrystallinity of Hirai's highly-oriented ferroelectric material is an inherent property. Hirai shows that the ferroelectric material is a highly-oriented thin-film showing a (001)-face (col.4/ll.50-52), but fails to specify that it is also polycrystalline or not amorphous. Nonetheless, (001)-PZT planes are polycrystalline (see remarks section below).

15. Regarding claim 17, Hirai shows that the polycrystalline film is greater than 100 angstroms (col.4/ll.42).

16. Regarding claim 18, Hirai shows that the buffer layer is a template to provide an oriented growth of the ferroelectric film (col.4/ll.31-35)

17. Regarding claim 19, Hirai shows that a dry-oxidation process comprising an oxygen-bearing compound may form the oxide layer (col.9/ll.58-61).

18. Regarding claim 20, Hirai shows that the oxide layer is silicon dioxide (col.9/ll.58). The substrate-surface passivation-property is an inherent property to Hirai's oxide layer. Hirai's oxide layer is made of silicon dioxide. However, Hirai fails to explicitly describe that the oxide layer passivates the surface of the substrate. Nonetheless, Hirai's oxide layer is characterized by its passivation effect on the surface of the substrate (see remarks section below).

19. Regarding claim 21, Hirai shows (see, *e.g.*, fig. 1) most aspects of the instant invention including a method for fabricating a non-volatile memory device, the method comprising:

- providing a substrate **1**

- forming a first buffer layer **4** overlying the substrate **1**
- forming a second buffer layer **5** overlying the first buffer layer **4**
- forming a ferroelectric material **6** overlying the substrate **1**
- forming a gate layer **7** overlying the ferroelectric material **6** and a channel region
- forming first and second doped regions **2, 3** adjacent to first and second ends of the channel region

Hirai (col.7/ll.37-44) also heats the substrate in an oxidizing atmosphere at a temperature of from 650-750°C. Hirai, however, fails to disclose this treatment as an annealing step that will enhance the alignment of crystallites of the buffer layer. Nonetheless, annealing is a thermal treatment carried out in order to eliminate various weaknesses, or to produce other qualities in a material. As taught by Kirlin (col.35/30-33) and Maiti (col.3/ll.33-36, col.4/ll.10-14), Hirai's heating step will remove the vacancies of the buffer layer. Although the prior art fails to explicitly describe that Hirai's heating step enhances the alignment of crystallites within the buffer layer, it is obvious that Hirai's thermal treatment would have the same claimed benefits since the same annealing step is used.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art that Hirai's heat treatment is an annealing step for the buffer layer, as taught by Kirlin and Maiti, that will reduce defects and enhance the alignment of crystallites within the layer.

20. Regarding claim 22, Hirai shows that the first buffer layer is a gate oxide layer (col.7/ll.38) and that the second buffer layer may be a MgO layer (col.2/ll.39).

21. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai, Kirlin, and Maiti in view of Yamazaki (US 6072724).

22. Regarding claim 2, Hirai/Kirlin/Maiti shows most aspects of the instant invention (see paragraphs 4-20 above) but fails to specify that the channel region be about 1 micron or less.

Yamazaki (col.2/ll.45-46), on the other hand, teaches that it is known that the channel length is an important design parameter that will determine the channel current of the transistor.

Consequently, it would be an obvious matter of design choice to select a suitable channel length for the transistor of Hirai/Kirlin/Maiti, as suggested by Yamazaki, since the channel length is a variable of importance subject to routine experimentation and optimization and it is not inventive to discover the optimum or workable ranges by routine experimentation.

23. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai/Kirlin/Maiti, as applied to claim 1 above, further in view of Van Zant and Evetts (US 5361720).

24. Regarding claim 11, Hirai/Kirlin/Maiti shows most aspects of the instant invention (see paragraphs 4-20 above), except for sputtering the buffer material from a substantially pure magnesium target to form a magnesium oxide layer. Hirai differently deposits the magnesium layer using vacuum evaporation (col.4/ll.10-12).

Van Zant (pp.412), however, teaches that there are several advantages to the use of sputtering over vacuum evaporation. One is the improvement in step coverage. Evetts (col.2/ll.15-20), on the other hand, teaches that sputter deposition from a magnesium metal target in a sputtering gas comprising oxygen is a preferred method of forming a high-quality MgO layer.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art to sputter Hirai/Kirlin/Maiti's buffer layer from a magnesium target to form the MgO layer, as suggested by Van Zant and Evetts, in order to improve the step coverage while forming a high-quality MgO layer.

25. Regarding claim 12, Hirai shows most aspects of the instant invention (see paragraph 4-20 above). In addition, Evetts (col.2/ll.2) shows that the deposition temperature may be as low as 540°C. Hirai/Kirlin/Maiti/Van Zant/Evetts, however, fails to teach a sputtering temperature between 400-500°C.

In spite of the above, generally, differences in temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation". *In re Aller*, 220 F.2d 454,456,105 USPQ 233, 235 (CCPA 1955).

There is no evidence supporting the claimed temperature range, *i.e.*, 400-500°C, as critical to the invention, and therefore it would have been obvious.

26. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai/Kirlin/Maiti/Van Zant/Evetts and Wolf.

27. Hirai/Kirlin/Maiti/Van Zant/Evetts shows most aspects of the instant invention (see paragraph 24 above). In addition, Hirai (col.7/ll.40-44) shows that the annealing may be performed at 750°C for 20 minutes. Hirai/Kirlin/Van Zant/Evetts, however, fails to perform the annealing between 800-1000°C for about 30 minutes.

Wolf (pp.57), on the other hand, teaches that it is known that temperature and time are important design parameters affecting wafer warpage or slip and dopant diffusion.

Consequently, it would be an obvious matter of design choice to select a suitable temperature and time for the anneal step of Hirai/Kirlin/Maiti/Van Zant/Evetts, as suggested by Wolf, since these are variables of importance subject to routine experimentation and optimization and it is not inventive to discover the optimum or workable ranges by routine experimentation.

In spite of the above, generally, differences in temperature and time will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation". *In re Aller*, 220 F.2d 454,456,105 USPQ 233, 235 (CCPA 1955).

There is no evidence supporting the claimed temperature range and time value, as critical to the invention, and therefore it would have been obvious.

28. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai/Kirlin/Maiti in view of Iyer (US 5629246).

29. Regarding claim 23, Hirai/Kirlin/Maiti shows most aspects of the instant invention (see paragraphs 4-20 above). Hirai (col.4/ll.49) also shows that the second buffer layer is a highly-oriented layer. Hirai/Kirlin/Maiti, however, fails to show that the first buffer layer is an amorphous layer.

Nonetheless, Hirai (col.7/ll.38) shows that the first buffer layer is a silicon-dioxide layer, which is used as a dielectric. As taught by Iyer (col.1/ll.16-20), silicon dioxides used as dielectrics in integrated circuits are typically amorphous materials.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time of the invention that Hirai/Kirlin/Maiti's first buffer layer is amorphous, as taught by Iyer, since this is a silicon dioxide layer used as a dielectric and silicon dioxides used as dielectrics in integrated circuits are typically amorphous.

30. Regarding claim 24, although Hirai does not show the second buffer layer having a thickness less than 10 nm, he shows that the first buffer layer may be approximately 14 nm (col.12/ll.3). Hirai's thickness appears to be closed enough to the claimed thickness range that one of ordinary skill in the art would have expected Hirai's layer to have the same properties as those of the claimed layer; consequently, it would have been obvious. *Titanium Metal Corp. of America v. Banner*, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985).

Moreover, it would be an obvious matter of design choice to have the second buffer layer having a thickness not greater than 10 nm, instead of 14 nm, since such a

modification would have involved a mere change in the size of the second buffer layer. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

31. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai/Kirlin/Maiti and Wolf.

32. Regarding claim 26, see the comments stated above in paragraph 27 with respect to claim 13, which are considered repeated here.

Remarks

33. As taught by Auciello (US 5453661/col.5/ll.7-25), the highly-oriented ferroelectric film of Hirai that mainly shows the X-ray (001)-diffraction peak is polycrystalline.

34. As taught by Van Zant (pp.154-155), silicon dioxide layers are characterized by its passivating effect over the surface of a substrate.

Response to Arguments

35. The applicant argues:

> Hirai merely discloses heating the substrate in an oxidizing atmosphere at a temperature of 650-750°C to form a silicon oxide film under the buffer layer. Hirai describes heating the substrate to form the silicon oxide film and is devoid of any teaching or suggestion of thermally annealing the buffer layer to enhance an alignment of crystallites of the buffer layer.

The examiner responds:

The references may suggest doing what an applicant has done even though those of ordinary skill in the art were ignorant of the existence of the problem (*In re Gershon*, 152 USPQ 602 (CCPA 1967)).

Annealing is a thermal treatment carried out in order to eliminate various weaknesses, or to produce other qualities in a material. As taught by Kirlin (col.35/ll.30-

33) and Maiti (col.3/ll.33-36, col.4/ll.10-14), Hirai's heating step will remove the vacancies of the buffer layer. Although the prior art fails to explicitly describe that Hirai's heating step enhances the alignment of crystallites within the buffer layer, it is obvious that Hirai's thermal treatment would have the same claimed benefits since the same annealing step is used.

Conclusion

36. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

37. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

38. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November

1989). The Art Unit 2814 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(703) 308-6558** and between the hours of 9:00 AM to 7:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

40. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

41. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/295, 438/3, 365/145	2/20/2003
Other Documentation: PLUS Analysis	9/11/2002
Electronic Database(s): EAST (USPAT, EPO, JPO)	2/20/2003

SUPERVISORY PRIMARY EXAMINER
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